ABSTRACT

A clamping circuit including a clamping diode, a bias line, and a clamp line is incorporated into a pixel circuit of amorphous silicon sensor arrays. The clamp diode in each pixel prevents the voltage across the photodiode from dropping below a specific threshold. By keeping the photodiode under reverse bias even under conditions that may otherwise saturate the pixel, image lag is reduced. In full fill factor amorphous silicon sensor arrays, a clamping circuit includes a clamp TFT, a bias plane, a clamp line, and a drain line. The clamp TFT reduces lag and blooming by draining off excess current developed under overexposure conditions. A method to globally reset a sensor array and a method to test and repair a TFT matrix in full fill factor sensor arrays without damaging the overlying collection electrode and sensor layer are also provided.